Lucas Martins Veras Pereira

Computer Engineer

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Campinas – São Paulo, Brazil
27 Years Old

Profile

As a curious and forward-looking person, I`ve worked on research projects related to SoC and Image processing using FPGA while in college, which led me to study more about microelectronics. I am a computer engineer with experience in designing and verifying digital systems, and my topics of interest are computer architecture, ASIC functional verification, and image processing.

Experience

Digital IC Verification Engineer – Eldorado Research Institute
Mar. 2023 – Present

Working on CPU verification and other IPs, my main activities are:

- Development of verification plans, testbenches and reference models
- Development of an in-house RISC-V reference Model
- Gate-Level simulations
- Usage of Verilog, SystemVerilog, SystemVerilog DPI with Python integration, and UVM

Senior Application Engineer – Cadence Design Systems
Mar. 2022 – Mar. 2023

As part of the System Verification Group, I work with cutting-edge IC emulation and prototyping tools to support customer needs.

- Check design compilation and runtime performance.
- Support customers with emulation verification environments
- Development of application`s features demonstration.
- Usage of Palladium and Protium platforms, Verilog, SystemVerilog, testbench acceleration architectures, UVM, and scripting languages.

Digital IC Verification Engineer – Eldorado Research Institute
Mar. 2020 – Mar. 2022

Working on verification of high-speed ASIC DSP where my main activities were:

- Development of verification plans
- Implementation of reference models in Python and SystemVerilog
- Scripting
- Usage of Verilog, SystemVerilog, SystemVerilog DPI with Python integration, and UVM

ASIC Design and Verification Trainee - IC Brazil Program
Apr. 2019 - Feb. 2020

I worked on several stages of the project flow of an integrated circuit. Among the activities I performed, the following stand out:

- Development of a USB device verification environment using the UVM methodology
- Design and hardware description of the configuration module for the USB protocol

Technical skills

- UVM and UVM-A Testbenches
- Testbench architecture
- Scripting Languages
- C/C++, and Python
- SystemVerilog and Verilog
- Computer architecture

- Versioning tools
- Linux
- EDA Tools
- Testbench Acceleration
- Verification Plan
- Emulation and Prototipation

Education

Computer Engineering - University of Vale do Itajaí
Itajaí – Santa Catarina, Brazil
2014 – 2018

As the final project, I implemented in FPGA (using Xilinx Tools) an accelerator for the CCSDS 123 prediction step for the compression of hyperspectral images.

Publications

A Low-Cost Hardware Accelerator for CCSDS 123 Predictor in FPGA
IEEE International Symposium on Circuits and Systems (ISCAS) · May 29, 2019

Analysis of LEON3 Systems Integration for a Network-on-Chip
IEEE Latin American Test Symposium · Mar 14, 2018